Noise Tolerant low-pass filter for IF processing

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ABSTRACT

This paper deals with a robust design of a FIR filter used in a digital downconverter for WLAN applications. As a result of the new trends in semiconductor technology using the new scale of integration, the current design tools and methodologies cannot provide a reliable medium for digital circuit implementation due to the existence of Deep Submicron (DSM) noise. Then, there are two groups of solutions to protect linear operations, such as FIR filters, from technology noise. The First one consists of protecting the data in operations, such as addition or multiplication, using coding theory. The second one treats the problem from an algorithmic point of view, which is known as Algorithmic Noise Tolerant (ANT). The most popular ANT for linear filters is known as Soft-DSP, which is based on a linear predictor to perform a parallel estimation of the filter output, understood as additional information to protect the original filter operation. This paper proposes an alternative algorithm for Parallel-Estimation ANT (PE-ANT) in which the original filter is partially duplicated. Simulation results show that this approach has better performance under bad noise conditions.

I. INTRODUCTION

The application of sophisticated digital signal processing techniques for communications, such as multi-user detection or smart antenna algorithms, imposes a stringent demand on hardware implementations. This increase on computational complexity requires the use of the new scale of integration in order to provide System on a Chip (SoC) solution. On the other hand, the current semiconductor technology, design tools and methodologies cannot achieve an enough level of noise-immunity so as to consider the new technologies as a reliable medium [1][2]. This situation leads to a new situation in communication systems, which should face both problems: the reliability of communication under noisy channel and reliability of computation in a unreliable medium.

The problem of guarantying a reliable computation with elements that themselves are unreliable was firstly analyzed in some times ago by Von Newman, Shannon and Moore from an information theory point of view [3][4]. Later, the equivalence between a reliable communication and a reliable computation was shown in [5]. This work leads with the introduction of the concept of computation capacity defined as the maximum rate for computing with an arbitrary high reliability. Recently, a mathematical basis to treat the problem from an information theoretic point of view, which has lead to solutions that are appropriate for digital signal processing, has been presented in [6].

During the last decades the solutions to achieve reliability can be divided in two big groups. The first one, which is called Algebraic Data Integrity (ADI), is based on the application of algebraic error protecting codes to the data operands. These codes are applied to linear operations such as addition or multiplication. Arithmetic Codes [7][8] and Redundant Residue Number System Codes [9][10] are approaches that belong to this group. The second group, known as Algorithmic Noise Tolerant (ANT), apply noise protection from an algorithmic point of view, without considering the error in each specific operation. In this case, the level of protection provided by the solution depends on the algorithm architecture. One of the main differences between both approaches is that ADI tries to protect all bits of the result in each single operation while ANT tries to keep the algorithm performance at an acceptable level.

ANT solution for digital FIR filters, known as Soft-DSP, is presented in [11]. This approach is based on the estimation of the filter output using linear prediction. Therefore, this solution can be classified in the group that addresses ANT by performing a parallel estimation of the filter output (PE-ANT). In this paper we propose a new algorithm for this group of solutions which deals with the duplication of some filter coefficients to achieve better performance, particularly when high level of noise is found in the technology elements.

The paper is organized as follows. Section II describes the concepts behind generic parallel estimation ANT and introduces the system model used in this work. Section III describes the previous work on Soft-DSP and in section IV the proposed PE-ANT is presented. Section V shows the results after applying both algorithms on a low pass digital filter used for IF downconversion in a WLAN system. Finally, section VI exposes the conclusions of the paper.

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II. PARALLEL ESTIMATION ANT

In order to highlight the advantages of the proposed solution, let's consider a FIR filter to be used in a digital downconverter. The filter is assumed to be implemented using an scale of integration in which the DSM Noise affects the reliability of the filter operation. The system is modelled as a reliable filter with noise added at the output of the filter. Since there is no statistic model of noise in DSM, the model used assumes that any bit of each output sample in the filter can be incorrect with probability P_{err}, [11]. Thus, the noise filter can be modelled by means of equation (1).

$$y_e(n) = y(n) + w(n) = \sum_{k=0}^{N-1} h(k) \cdot x(n-k) + w(n) \quad (1)$$

x(n) denotes the input signal, *y(n)* is the noiseless output signal, $y_e(n)$ is the noise affected output, *h(n)* are the filter coefficients, *N* is the number of taps of the filter and *w(n)* represents the equivalent DSM noise at the output of the filter.

As for the case of communication systems, the noise level can be expressed as the Signal-to-Noise Ratio (SNR) at the output of the filter. Therefore the main goal of ANT algorithms is to maintain the output SNR to an acceptable level for each application.

Fig. 1. shows the system model for a generic (PE-ANT) solution. This technique performs an estimation of the filter output. The data used for error estimation can be either the previous filter output, the filter input signal or both. Then, the estimated output, $y_p(n)$, and the noise-added output are processed in the error control block to provide a noise protected sampled. Notice that for several DSP applications the output is not completely free of error, but it must keep the signal-to-noise ratio at an acceptable level depending on each application. Therefore the error control block is designed to increase the SNR at filter output, $y_e(n)$. Notice also that the estimator is assumed to be free of error. This assumption is feasible by using redundant ADI or simply circuit replication techniques for error protecting as long as the complexity of the estimator could be maintained lower than the original filter.

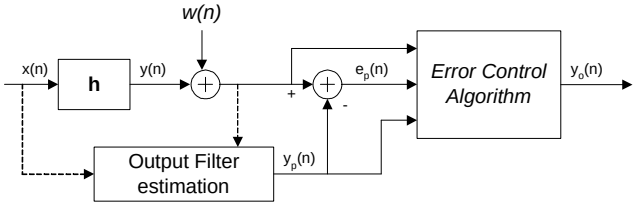

Fig. 1. Parallel Estimation ANT.

III. SOFT-DIGITAL SIGNAL PROCESSING

Soft Digital Signal Processing is a parallel estimation ANT algorithm in which the estimation is based on a linear prediction. Therefore the estimation is based just on the previous filter output. Fig. 2 shows the scheme applied in Soft-DSP ANT. In digital communication systems the signal is usually correlated and thus, the low-pass filtering of these signals generates a process that can be easily predicted using a low order predictor [12]. Equation (2) denotes the expression of the predictor output.

$$y_p(n) = \sum_{k=0}^{NP-1} y_e(n-k) \cdot p(k) \quad (2)$$

where *p(k)* are the predictor coefficients and *NP* is the predictor order. The predictor coefficients are calculated to minimize the mean squared error (MMSE) between the noiseless filter output, *y(n)*, and the predictor.

Notice that the last *NP* samples of the filter output are assumed to be correct in order to have good signal estimation which is based on the prediction operation. Since this assumption is not necessarily valid for a system with noise coming from the used technology, Soft-DSP includes an error control algorithm to reduce the effect of error propagation for the case when an error occurs in the filter output. In this situation equation (3) denotes the estimation error.

$$\hat{e}_p(n) = w(n) + e_p(n) \quad (3)$$

where $\hat{e}_p(n)$ represents the total estimation error, $e_p(n)$ is the prediction error and *w(n)* is the error introduced by DSM noise. Assuming that there are no DSM errors for the next *NP* samples the equation (3) can be expressed in vector form as follows:

$$\hat{\mathbf{e}}_p(n) = w(n) \cdot \mathbf{p} + \mathbf{e}_p(n) \quad (4)$$

where

$$\hat{\mathbf{e}}_\mathbf{p}(n) = \left[\hat{e}_p(n) \quad \hat{e}_p(n+1) \quad \cdots \quad \hat{e}_p(n+NP)\right]^T$$
$$\mathbf{p} = \left[1 \quad -p(1) \quad -p(2) \quad \cdots \quad -p(NP)\right]^T$$
$$\mathbf{e}_\mathbf{p}(n) = \left[e_p(n) \quad e_p(n+1) \quad \cdots \quad e_p(n+NP)\right]^T$$

Given Equation (4), the error control algorithm defined in Soft-DSP is described in the following lines:

- Let σ_p^2 be the variance of the prediction error with noiseless digital filter.
- An error is detected if
$$\left|\mathbf{p}^T \cdot \hat{\mathbf{e}}_p(n)\right| > s_p^2 \quad (5)$$
- If an error is detected $y_o(n) = y_p(n)$ else $y_o(n) = y_e(n)$

Notice that the performance of Soft-DSP depends on the decision threshold for error detection and on the assumption that $y_e(n)$ is relatively large compared to $y_p(n)$. This forces to know a priori the statistics of the error magnitude and then fix an adequate threshold to achieve the required performance. Unfortunately, in practice this knowledge is not always available.

Another important limitation of this approach is that the performance of the ECA deteriorates when multiple error occurs in a span of *2·NP* samples of the original filter. As a consequence of this limitation, this algorithm can only be applicable when the frequency of errors in the original filter is less than $1/(2\times NP)$.

To finish the comments on Soft-DSP algorithm notice that the complexity required to carry out the error detection and correction is *2·NP* operations, taking into account both of them, the predictor filter and the error control computations.

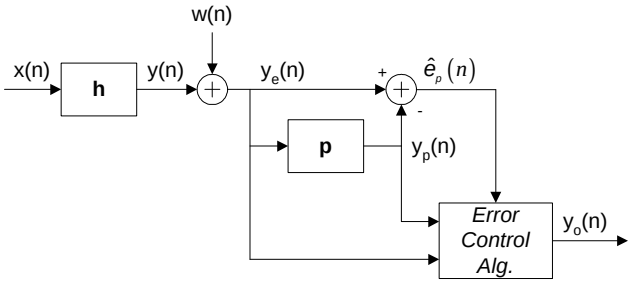

Fig. 2. Soft-DSP scheme**.**

IV. PARTIAL FILTER DUPLICATED PREDICTION

The main problem of Soft-DSP algorithm is to take control of the error when it is propagated through the predictor taps. The Error Control Algorithm (ECA) contemplated by Soft-DSP solution reduce this effect when the error occurs at a rate larger than *2·NP*. Therefore, in the presence of high level of DSM noise the ECA cannot take control over all possible errors, particularly when two or more errors occurs in a span of *2·NP* consecutive output samples.

The first approach considered in this work is to reduce the predictor order to have just one coefficient and thus improve the estimator variance by duplicating part of the filter. Fig. 3 shows the proposed Partial Filter Duplicated ANT (PFD-ANT). The symbol D^{-k} represents a k-sample delay, which is introduced to synchronise the estimated signal with the output filter. In this approach the output filter estimation is generated by the addition of two signals: the output of the partially replicated filter and a linear prediction, which order is one. The duplicated filter coefficients should be those with maximum absolute value. In that way, a better estimation performance is obtained.

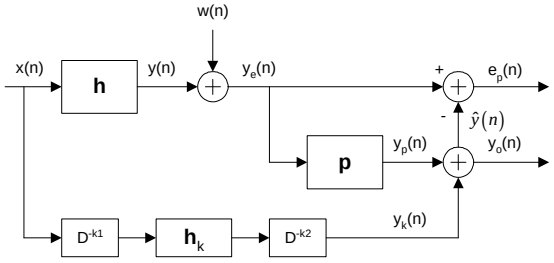

Fig. 3. Partial Filter Duplicated ANT.

The estimated signal can be expressed as in equation (6).

$$\hat{y}(n)=\sum_{j=k}^{k+L-1} h(k)\cdot x(n-k)+a\cdot y_e(n-1) \qquad (6)$$

where *k* and *L* are respectively the first tap of the original filter and the number of coefficients to be duplicated. *a* denotes the predictor tap which is calculated for minimizing the minimum squared error (MMSE) between the estimated signal and the noiseless filter output as shown in the following equations,

$$e_y(n)=y(n)-\hat{y}(n) \qquad (7)$$

$$a=\frac{1}{r_y(0)}\cdot\left(r_y(1)-\mathbf{r}_{yx}^{T}\cdot\mathbf{h}_k\right) \qquad (8)$$

where

$$\mathbf{r_{yx}}=\left[r_{yx}(-k)\quad r_{yx}(-k+1)\quad\cdots\quad r_{yx}(-k+L-1)\right]^T \qquad (1.1)$$

$$\mathbf{h_k}=\left[h(k)\quad h(k+1)\quad\cdots\quad h(k+L-1)\right]^T \qquad (1.2)$$

In this case the predictor order is reduced to one coefficient and thus, the ECA can be simplified or even eliminated because the effect of error propagation is highly reduced. In fact, as shown in section V, in practical situations the estimated output has a noise level that can be tolerated in many digital signal processing applications. Finally In terms of complexity the PFD-ANT requires *L+1* computations.

V. APPLICATION ON DIGITAL LOW-PASS FILTER

The application of PFD-ANT is performed in a filter used in a digital downconverter for WLAN systems. The number of coefficients of the original filter is 23. For noise modelling it is assumed that any bit of each output sample can be incorrect with probability of error, P_{err}. In the

simulations P_{err} ranges between 10^{-1} and 10^{-5} to force different signal to noise ratio at the output of the original filter. In order to evaluate the gain of the proposed PFD-ANT the noise model allows burst errors and thus, is not limited to have low frequency errors, as it is required by Soft-DSP algorithm.

The number of coefficients to be duplicated in PFD-ANT is set to assure that the signal $y_k(n)$ contributes with an estimation of about the 70% of the original output. Fig. 4 shows the error variance of partial filter duplicated as a function of the duplicated taps. It is shown that the error variance becomes relatively small when at least the three taps with maximum absolute value are duplicated.

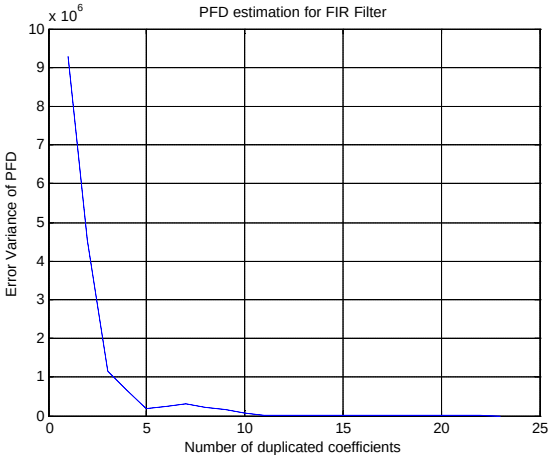

Fig. 4. Error variance of partial duplicated filter output

Fig. 5 depicts the final output SNR applying both of them, Soft-DSP and PFD-ANT. The result is presented as a function of the SNR due to the DSM noise in the original filter without any compensation, which will be referred as original SNR for the rest of this paper. In this simulation the input signal is quantified using 6 bits. In this simulation the order of the predictor in Soft-DSP is set to $NP = 3$ and the number of duplicated coefficients in PFD-ANT is $L = 3$. Notice that, in this case, the complexity of PFD-ANT is 4 operations while the complexity of Soft-DSP is 6 operations.

The simulation results show that PFD-ANT improves the output SNR even with negative values of the original SNR while Soft-DSP cannot offer significant improvements for original SNR below 10dB. This is because in the range below 10dB the probability that two or more errors occurs in a span of $2 \cdot NP$ becomes relevant. In contrast, notice also that PFD-ANT keeps constant the output SNR and does not offer improvements for high original SNR.

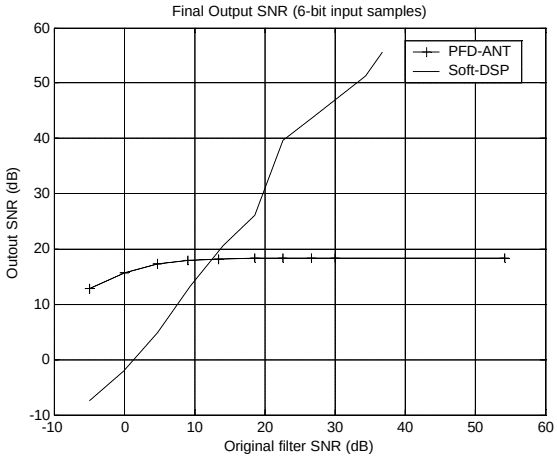

Fig. 5. Comparison between Soft-DSP (NP = 3) and PFD-ANT (L = 3). Input signal is quantified using 6 bits.

Fig. 6 shows the result of the same simulation when the input signal is quantified using 10 bits. Assuming that there is not truncation nor rounding in hardware implementation, the bit-width at the output of the original filter is larger than the previous simulation. Since a sample is erroneous when one or more bits are incorrect, the probability of error of output filter samples is higher than in the previous case. Therefore, the probability that two or more errors occurs in a span of $2 \cdot NP$ samples is also higher. As a consequence the performance of Soft-DSP approach is deteriorated with respect to the previous simulation. However, notice that PFD-ANT scheme maintains the performance given a more robust solution to those cases in which the achieved output SNR can be allowed.

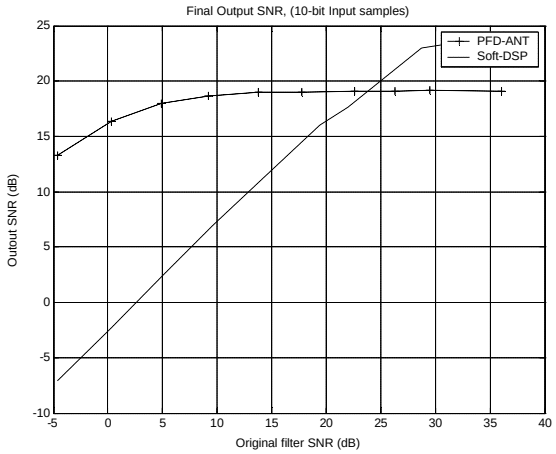

Fig. 6. Comparison between Soft-DSP (NP = 3) and PFD-ANT (L = 3). Input signal is quantified using 10 bits.

VI. CONCLUSIONS

The future trends in semiconductor technology, that contemplates the reduction of the scale of integration,

cannot assure a reliable medium to implement digital systems due mainly to the effects of Deep Submicron (DSM) noise. This paper has presented the design methodology of a FIR filter which is robust against DSM noise. The solution proposed is based on Algorithmic Noise Tolerant (ANT) strategies applied to digital signal processing applications known as Soft-DSP. The proposed system, called Partial Filter Duplication ANT (PFD-ANT) protects the original filter by performing an estimation of the filter output. In particular, the presented solution performs an estimation based on linear prediction of order one and partial duplication of the original filter coefficients. The duplicated taps must be those with the highest absolute value. A low-pass filter used in a digital downconverter affected with DSM noise is simulated to test the performance of PFD-ANT. Simulation results show that in the presence of a SNR at the output of the original filter below 15dB, the final output SNR keeps a minimum value of about 18dB, which can be considered good enough in many situations of digital communication systems. Simulations also show that PFD-ANT maintains the performance when burst errors occurs at the output of the original filter, giving a robust solution for a bad conditioned environment.

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